Top-Gated Graphene Field-Effect Transistors with High Normalized Transconductance and Designable Dirac Point Voltage

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ABSTRACT High-performance graphene field-effect transistors (G-FETs) are fabricated with carrier mobility of up to 5400 $cm^2/V \cdot s$ and top-gate efficiency of up to 120 (relative to that of back gate with 285 nm SiO_2) simultaneously through growing high-quality Y_2O_3 gate oxide at high oxidizing temperature. The transconductance normalized by dimension and drain voltage is found to reach 7900 $\mu F/V \cdot s$, which is among the largest of the published graphene FETs. In an as-fabricated graphene FET with a gate length of 310 nm, a peak transconductance of 0.69 $mS/\mu m$ is realized, but further improvement is seriously hindered by large series resistance. Benefiting from highly efficient gate control over the graphene channel, the Dirac point voltage of the graphene FETs is shown to be designable *via* simply selecting a gate metal with an appropriate work function. It is demonstrated that the Dirac point voltage of the graphene FETs can be adjusted from negative to positive, respectively, *via* changing the gate material from Ti to Pd.

KEYWORDS: graphene · field-effect transistor · transconductance · Dirac point voltage

Graphene is considered as a promising material for high-performance nanoelectronics due to its extremely high carrier mobility, the ultimate thin body, and stability.[1−5] Because of the lack of an intrinsic band gap,[2,3] graphene is believed to be more suitable for radio frequency (RF) analog electronics,[4,5] instead of digital applications where a large current on/off ratio is required. Recently, graphene field-effect transistors (G-FETs) with a cutoff frequency (f_T) of up to 100−300 GHz were successively fabricated,[6,7] and their advantages for RF applications were amply demonstrated. Besides f_T, there are some other device parameters that are also important and need to be optimized. These parameters include transconductance and the working point of the device, that is, the Dirac point voltage. The transconductance of a transistor represents the amplifying ability which is very important for, among others, signal and power amplifier and frequency doubler applications,[8−10] and the Dirac point voltage will affect the dc supply voltage needed in real applications.[8−10] It is well-known that the quality of the gate oxide is one of the key factors determining the transconductance of a real device, and a high-quality dielectric layer is therefore highly desirable on pristine graphene which could lead to both high carrier mobility (less scatters) and large gate capacitance. Several dielectrics have been successfully grown on graphene *via*, for example, depositing functionalization and buffering layers to reduce scattering and retain high mobility, but the additional buffering layers significantly increase the effective thickness of the gate dielectric layer and reduce the gate oxide capacitance.[11−18] Very recently, an ultrathin yttrium oxide layer was grown on graphene with an equivalent oxide thickness (EOT) of about 1.5 nm and an extremely large oxide capacitance of more than 2.2 $\mu F/cm^2$.[19−21] However, mobilities for both electron and hole were found to be lower than 2000 $cm^2/V \cdot s$.[19−21] It is the aim of this paper to report a simple annealing procedure that simultaneously yields a high carrier mobility of more than 5000 $cm^2/V \cdot s$ and large gate capacitance of about 1.5 $\mu F/cm^2$.

Although it is well-known that the position of the Dirac point is affected by work function of the contact metal in back-gated graphene FETs,[22] few works focused on controlling the Dirac point of top-gated graphene FETs, which is another significant parameter for FET, similar to threshold voltage in conventional FETs. Similar to carbon nanotube FETs,[23] effective and stable doping is not easy in graphene, and the Dirac voltage of graphene FETs cannot thus be readily adjusted by tuning the dopant density of the graphene channel as in silicon

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MOSFETs.[24] Alternatively, the Dirac point of a graphene device may be adjusted by selecting a gate metal with suitable work function, but an important precondition for realizing this potential is to have a large gate capacitance to ensure a strong coupling between the gate electrode and graphene channel.

In this paper, we fabricated a high-performance graphene FET with a carrier mobility of up to 5400 $cm^2/V \cdot s$ and a top-gate relative efficiency of up to 120 (relative to the back gate with 285 nm SiO_2) simultaneously, leading to a normalized transconductance (by dimension and drain voltage) as large as 7900 $\mu F/V \cdot s$, which is among the largest in the published devices. In an as-fabricated graphene FET with a 310 nm gate length, a peak transconductance as high as 0.69 mS/μm is realized. One of the important merits of a highly efficient gate control over the graphene channel is further demonstrated by using gate metals with appropriate work functions to adjust the Dirac point voltage of the graphene FETs. It is shown that using titanium instead of palladium as gate metal the Dirac point voltage of the graphene FETs can be adjusted from negative to positive, respectively; that is, the type of charged carriers in the channel at zero gate voltage can be shifted from electrons to holes.

RESULTS AND DISCUSSION

Figure 1a shows the structure of the top-gated graphene FET, and Figure 1b shows the SEM picture of an as-fabricated device in which the graphene channel is covered by a gate of about 1 μm in length and 2.7 μm in width. In order to improve the quality of the Y_2O_3 gate insulator, the yttrium (Y) film was oxidized at 270 °C, which is higher than the previously used oxidization temperature of 180 °C.[19-21] To avoid possible deformation of graphene caused by O_2 at high temperature,[25] the oxidization temperature was therefore chosen to be less than 300 °C. In order to extract the carrier mobility using the diffusive model, devices used in this work were fabricated with a relatively long gate length of about 1.0 μm. A typical transfer characteristic measured from such a device is shown as the inset of Figure 1c at a bias of 50 mV; from this curve, the relation between total resistance and top-gate voltage was then obtained and is shown in Figure 1c. The device is a typical ambipolar FET as manifested by the "V" shape gate dependence of the transfer characteristics on the gate voltage. To extract carrier mobility from transfer characteristics, the oxide capacitance of the top gate must be obtained at first. Since the graphene channel can be simultaneously controlled by top gate and back gate, the shift in the top-gate Dirac point voltage $V_{TG,Dirac}$ is linearly dependent on the change of the back-gate voltage V_{BG} as shown in Figure 1d. The inverse of the slope of the $V_{TG,Dirac}-V_{BG}$ line is 121, which is determined by the ratio between

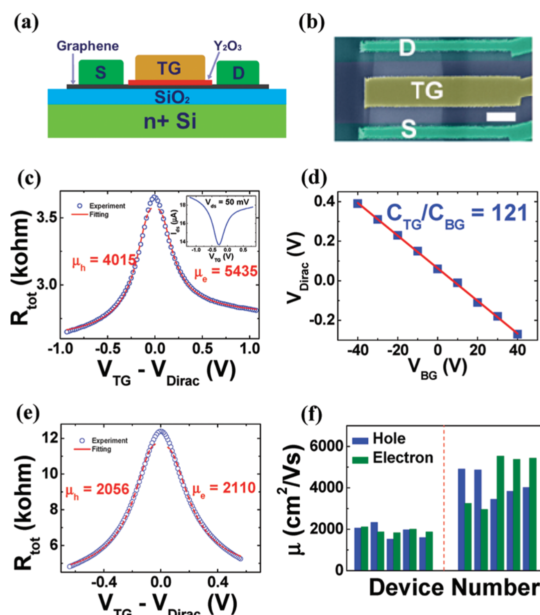

Figure 1. Electrical characteristics of graphene FETs. (a) Cross section diagram of the graphene FETs. (b) SEM image of an as-fabricated device. The channel length is about 2.6 μm, and gate length is about 1 μm. Scale bar: 1 μm. (c) Total resistance of the device under drain voltage of 50 mV. The blue circles show the experiment data with respect to Dirac point voltage; the red lines are theoretical fittings for hole and electron branches. The inset shows the as-measured drain current as a function of gate voltage. (d) Top-gate Dirac point voltage as a function of back-gate voltage. (e) Total resistance of a similar graphene FET with the dielectric being grown at 180 °C. (f) Statistics of carrier mobility of graphene FETs. Mobility of graphene FETs with Y_2O_3 dielectric layer formed at 180 °C is shown at the left side of the red dashed line; the right side shows mobility of graphene FETs with Y_2O_3 dielectric layer formed at 270 °C.

the top-gate oxide capacitance and back-gate capacitance of unit area, and is independent of the quantum capacitance of graphene, that is, $C_{OX}/C_{BG} = -\Delta V_{BG}/\Delta V_{TG}$.[13,15,16,19,20] Using a relative dielectric constant of 3.9 and a thickness of 285 nm for the back-gate silicon dioxide, which yields a back-gate capacitance 0.0121 $\mu F/cm^2$, the top-gate capacitance is derived to be 1.46 $\mu F/cm^2$. The value of top-gate capacitance can also be estimated by using the conventional capacitance equation, $C_{OX} = \kappa\varepsilon_0/t_{OX}$. For the Y_2O_3 film in the G-FET of Figure 1d, the oxide thickness t_{OX} is 6 nm (as measured by AFM) and the relative dielectric constant $\kappa \approx 10$.[20] We then obtain C_{OX} = 1.48 $\mu F/cm^2$, which is very close to the value of 1.46 $\mu F/cm^2$ that we just obtained. The electron mobility μ_e and hole mobility μ_h of the device are then extracted using the previously reported model[14]

$$R_{total} = R_s + \frac{L_G}{W}\frac{1}{e\mu\sqrt{n_0^2 + n^2}} \qquad (1)$$

where $R_{total} = V_{ds}/I_{ds}$ is the total resistance of the graphene FET including the series resistance R_s and the ideal channel resistance modulated by the top gate; L_G is the length of the top gate, and W is the width

of the graphene channel covered by the top gate; n and n_0 are the top-gate-modulated carrier density and the residual density, respectively, and e is the electron charge. The capacitive carrier density n is related to the gate voltage *via* the equation

$$V_{TG} - V_{TG,\,Dirac} = \frac{ne}{C_{OX}} + \frac{\hbar v_F \sqrt{\pi n}}{e} \quad (2)$$

where the first term on the right-hand side of eq 2 describes the carrier density induced by the top gate *via* C_{OX}, the second term describes the effect of quantum capacitance in graphene, and the Fermi velocity $v_F = 1.15 \times 10^6$ m/s.[3,18,20,26] It should be noted that the p-type branch and n-type branch are always asymmetric at two sides of the Dirac point in our devices, which was observed also in previous works[27−31] and attributed to the pinning of charge density below the contact metal[27,28] and the conductance suppression of only one carrier type induced by long-range scatters at the interface of the oxide/graphene.[29−33] Because of the conductance asymmetry, the hole branch and electron branch in the transfer characteristic are fitted separately using eqs 1 and 2, and corresponding hole and electron mobilities are extracted. The fitting yields a mobility of 4000 $cm^2/V \cdot s$ for holes and 5400 $cm^2/V \cdot s$ for electrons. The improved carrier mobility relative to previous G-FETs[19−21] with Y_2O_3 gate insulator is largely benefited from the use of higher oxidization temperature. Since the charged traps originated from defects will decrease with increasing oxidation temperature, scattering then decreases, leading to higher carrier mobility. Figure 1e gives the transfer characteristic of a typical G-FET with Y_2O_3 insulator oxidized at 180 °C, from which the carrier mobilities are extracted, which are, respectively, 2056 and 2110 $cm^2/V \cdot s$ for electrons and holes. To ensure the effect of oxidizing temperature on the quality of the Y_2O_3 insulator, we compared the carrier mobility between two groups of G-FETs in Figure 1f with the Y_2O_3 being formed at different oxidizing temperature. The carrier mobility ranges from 1500 to 2000 $cm^2/V \cdot s$ for the G-FETs fabricated with Y_2O_3 oxidized at 180 °C, which increases to about 3000−5500 $cm^2/V \cdot s$ for the G-FETs being fabricated with Y_2O_3 oxidized at 270 °C. The carrier mobility is thus seen (Figure 1f) to have been improved significantly both for electrons and holes simply *via* increasing the oxidization temperature from 180 to 270 °C.

Compared to the previously reported data, our graphene FET preserves both high mobility and gate efficiency, which in turn leads to high transconductance of a graphene device. Transconductance is the key device parameter which characterizes the amplifying ability of a FET device and is especially important for analog applications. It is well-known that the transconductance of a G-FET is dependent on its dimension and the source drain bias voltage. Although many G-FETs with large transconductance normalized only by channel width were reported,[13−18] a fair comparison between different devices is still absent since these devices were measured at different source/drain bias and channel length or electrical field. Unlike in conventional FETs, current saturation is not usually observable in graphene FETs and transconductance generally increases with increasing bias. Here we propose to use a normalized transconductance, by both channel width and field, to benchmark the amplifying ability of graphene FETs. For a FET with a long enough channel and in its linear working region,[24] transport of the device can be described using a drift-diffusion model, and the intrinsic transconductance can be written as

$$g_m = \mu C_{TG} \frac{W}{L_G} V_{ds} \quad (3)$$

in which W and L_G are, respectively, the width and length of the gate, C_{TG} is the gate capacitance, and μ is the carrier mobility. Normalized by the dimension and bias of the device, the transconductance is then related directly to the product of carrier mobility and gate capacitance

$$g_{mN} = g_m \frac{L_G}{W V_{ds}} = \mu C_{TG} \quad (4)$$

that is, the product of mobility and gate capacitance is a universal parameter for benchmark of the amplifying potential of graphene FETs with different dimensions and under various work voltages. Here we thus call it normalized transconductance. It should be noted that C_{TG} is the total capacitance due to two capacitors connected in series, that is, the oxide capacitor of the gate oxide and quantum capacitor of the graphene channel. It should be noted that the quantum capacitance of graphene is dependent on gate voltage and is usually much larger than the oxide capacitance especially at bias far from the Dirac point. As a simple approximation, therefore, we substitute C_{TG} with C_{OX} in eq 4. Table 1 lists three parameters including carrier mobility, gate capacitance, and normalized transconductance for our and other published high-performance G-FETs.[13−18] Although the mobility of our G-FET is not

TABLE 1. Comparison of Maximum Carrier Mobility and Gate Oxide Capacitance between Our Device and Other Published Graphene FETs (Data for Devices A−F Were Taken from References 13−18)

	μ ($cm^2/V \cdot s$)	C_{TG} ($\mu F/cm^2$)	μC_{TG} ($\mu F/V \cdot s$)
device A[13] (Columbia)	1200	0.552	662
device B[14] (UT, Austin)	8600	0.306	2632
device C[15] (IBM)	7700	0.184	1417
device D[16] (UCLA)	23600	0.164	3870
device E[17] (HRL)	6000	0.170	1020
device F[18] (Manchester)	10000	0.470	4700
this work	5400	1.462	7895

extremely high, the normalized transconductance can reach up to about 7900 μF/V·s, among the largest of the published graphene FETs.[34] The high normalized transconductance indicates the overall high efficiency of graphene channel and gate oxide. This normalized transconductance value suggests that, for a G-FET with a gate length of 1 μm and a bias of 1.0 V, its transconductance could reach up to 7.9 mS/μm, which is far above all of the published results for G-FETs with shorter gate length and larger bias voltage.[13−19,35,36] Except for the graphene channel and gate insulator, the series resistances including access resistance (from the graphene channel between top-gate and source/drain electrode) and contact resistance would also play an important role in G-FETs;[36−38] in particular, a large series resistance will seriously degrade the actual transconductance.

In general, the combination of high mobility and high gate efficiency will lead to a high transconductance in G-FETs. According to eq 3, the transconductance of a G-FET is inversely proportional to gate length L_G. The transconductance of the G-FET can thus be further improved by scaling down the gate length in graphene FETs. The process of fabricating G-FET with submicrometer channel and gate length is basically the same as mentioned above, but with a slight difference in the choice of source and drain contact metals. Here a more complex Ti/Pd/Au (1/20/30 nm) structure is used, aiming to further decrease the contact resistance.[6] Shown in Figure 2a are transfer characteristics of a graphene FET with gate length of about 310 nm and spacing between the top-gate electrode and source/drain contacts of about 100 nm. The on-state current reaches up to 1 mA/μm, which is among the largest in all reported graphene FETs.[6,7,9,13−18] The small I_{on}/I_{off} ratio of about 1.5 can be attributed to the relatively low fraction (~0.6) of the gate-modulated channel length compared to the total channel length. Figure 2b shows the transconductance per channel width, which is seen to strongly depend on the gate voltage owing to the impact of series resistance.[15,36,37] The peak transconductance is also dependent on source/drain bias, as shown in Figure 2c, which reaches up to 0.69 mS/μm at a bias of −2.0 V. This value is the largest observed in all non-self-aligned graphene FETs[6,9,10,13−18] and is about two times better than the silicon transistor with similar gate length.[39] To estimate the mobility and series resistance of this device, the V_{TG} dependent total resistance of the device is measured at low bias of 50 mV and shown in Figure 2d. The $R_{total}-V_{TG}$ curve is fitted using eq 1, yielding a hole mobility of 4936 cm^2/V·s (the corresponding normalized transconductance is about 7000 μF/V·s) and series resistance R_s of 815 Ω. Although a high peak transconductance of up to 0.69 mS/μm is achieved, the corresponding normalized transconductance is only about 45 μF/V·s, which it is much lower than its intrinsic value

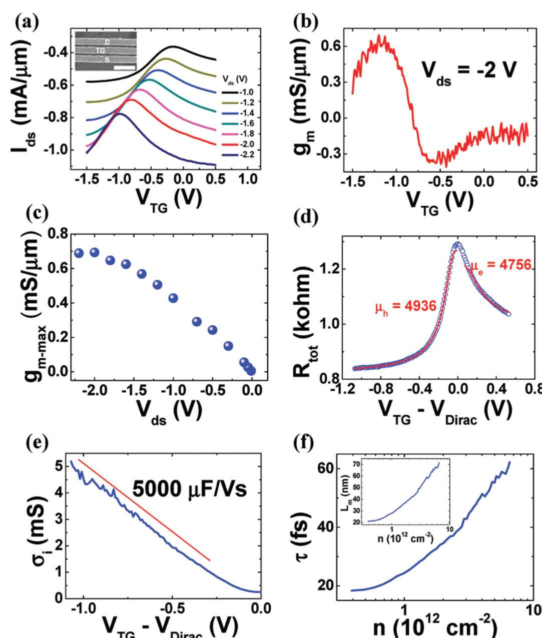

Figure 2. Electrical characteristics of a short channel graphene FET. (a) Transfer characteristics of a graphene FET with L_G = 310 nm at different drain bias. Inset shows the SEM image of the graphene FET. Scale bar: 1 μm. (b) Transconductance of the device as a function of top-gate voltage under a bias of −2.0 V and (c) peak transconductance of the graphene FET as a function of drain voltage. (d) Total resistance of the device as a function of gate voltage under drain voltage of 50 mV. The blue circles show the experiment data with respect to the Dirac point voltage; the red lines are theoretical fittings. (e) Gate-voltage-dependent conductivity of the channel after subtracting the series resistance. The slope of the curve is related to the normalized transconductance. (f) Scattering time as a function of carrier concentration in the G-FET. Inset shows carrier concentration-dependent mean-free-path length.

of 7000 μF/V·s. The tremendous gap between the actual normalized transconductance and the expected value results mainly from the existence of the large series resistance in the graphene channel which cannot be modulated by the top gate. If we subtract the series resistance *via* $R_{intrinsic} = R_{total} - R_s$ from the experimental data of Figure 2d, the conductance of the device is shown to follow V_{TG} almost linearly (Figure 2e), and the slope is just the normalized transconductance. It should be noted that the series resistance R_s is treated as a fixed value here. Since R_s originates from the part of the channel that is ungated by the top gate and contacts, it is, in general, dependent on the bias of the back gate[14] and nearly independent of the top gate. Since, in the device of Figure 2d, back gate is not used, it is reasonable to consider R_s as a fixed value. Then after eliminating the effect of series resistance, the normalized transconductance is recovered up to about 5000 μF/V·s, which is close to the intrinsic value of about 7000 μF/V·s, with the remaining difference being mainly a result from the effect of quantum capacitance. Therefore, the peak transconductance can be significantly improved through

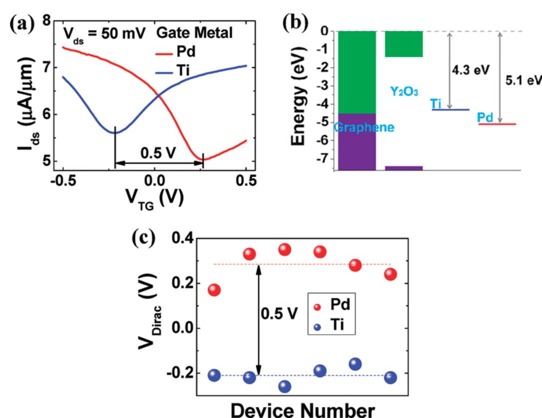

Figure 3. Dirac point voltages of graphene FETs with different top gate metals. (a) Transfer characteristics of two different devices with Ti and Pd being the gate metal. (b) Work function comparisons between graphene and Ti/Pd metal. (c) Statistics on the Dirac point voltage of 12 devices with Ti or Pd being gate metals.

decreasing the series resistance, which could be achieved by optimizing the contact and adopting a self-aligned gate structure to decrease access resistance. Very recently, G-FETs with ultrahigh transconductance were fabricated with self-aligned gate, and the major progress comes mainly with significantly lowered access resistance.[7] It should be noted that here the carrier mobility and series resistance of the G-FET are calculated using eq 1, which is based on the validity of the diffusive transport model, and we now consider the validity of using the diffusive model in our G-FET. The scattering time τ and mean-free-path length (MFP length) L_m of carriers are estimated as[30] $\tau = \sigma (\pi/n)^{1/2} \times \hbar/(e^2 v_F)$ and $L_m = v_F\tau$. The results are shown in Figure 2f. The MFP length is seen to increase with increasing carrier density but is smaller than 60 nm for relatively high $n = 6 \times 10^{12}$/cm^2 and is about 1/5 of the gate length. It is thus justified to use the diffusive transport model to analyze the results obtained from our G-FET.

The Dirac point voltage will affect the dc supply voltage needed in real applications and therefore is a significant parameter for G-FET operation. Similar to carbon nanotube FETs,[23] the Dirac point voltage of a G-FET cannot be readily adjusted by tuning the dopant density of the graphene channel as routinely done in silicon MOSFETs. This is because stable and controlled doping in graphene is difficult.[24] Benefiting from the excellent gate control over the graphene channel in our devices with ultrahigh gate capacitance, the Dirac point voltage can be adjusted by selecting appropriate gate metal with suitable work function. Figure 3a shows two typical transfer characteristics measured from two devices with a Ti and Pd gate. Typical hysteretic characteristics of the devices are given in the Supporting Information, which shows that only a 10 mV hysteresis exists when sweeping the top-gate voltage from −0.5 to 0.5 V and then backward. The Dirac point voltage V_{Dirac} is −0.22 V for the G-FET with a Ti gate, which increases to 0.27 V when using Pd as gate metal. A shift of up to 0.49 V in the Dirac point voltage is realized simply by changing the gate metal. At zero gate voltage, the device with a Ti gate is electron accumulated, and the device with a Pd gate is hole accumulated. This is in qualitative agreement with the work function difference between the gate metals. As shown in Figure 3b, the work function of Ti (W = 4.3 eV) is smaller than that of graphene (4.5 eV); that is, the Fermi level of Ti is higher than that of graphene, then the Fermi level of graphene will be raised after intimately contacting with the Ti gate through Y_2O_3 film as a media, and the channel would be electron accumulated. On the other hand, Pd (W = 5.1 eV) gate has a lower Fermi level than graphene, then the graphene channel would be a hole conductive one. The gate metal work function induced V_{Dirac} change is further manifested in the statistic results on 12 G-FETs (Figure 3c), among which 6 devices are fabricated with a Ti gate and the others with a Pd gate. For the devices with a Pd gate, the Dirac point voltage varies from 0.18 to 0.35 V, while for the devices with a Ti gate, the Dirac point voltage varies from −0.15 to −0.25 V. There exists clearly a gap between the two groups of devices, and the statistical Dirac point voltage shift here is about 0.5 V, which is smaller than the work function difference of 0.8 eV between Ti and Pd. This large discrepancy is largely due to the fact that the work function of a metal on a real dielectric is different from that in vacuum. As a rule, the effective work function difference between different metals on a dielectric is smaller than that in vacuum.[40,41] The ratio between the effective work function difference for different metals on a dielectric to that in vacuum is measured by a S parameter that accounts for dielectrics screening and depends on the electronic component of the dielectric constant[40,41]

$$\Phi_{M,eff} = \Phi_{CNL,d} + S(\Phi_{M,vac} - \Phi_{CNL,d}) \quad (5)$$

where $\Phi_{M,eff}$ is the effective work function of metal in dielectric, $\Phi_{CNL,d}$ is the charge neutrality level of the dielectric, and $\Phi_{M,vac}$ is the work function of metal in vacuum. Thus we have

$$\Delta\Phi_{M,eff} = S\Delta\Phi_{M,vac} \quad (6)$$

Since $\Delta\Phi_{M,eff}$ and $\Delta\Phi_{M,vac}$ are about 0.5 and 0.8 eV, respectively, we therefore obtain $S \sim 0.6$ for the metals on Y_2O_3 with a dielectric constant of about 10.

CONCLUSION

In conclusion, high-performance top-gated graphene FETs (G-FETs) have been fabricated with ultrahigh gate efficiency of up to 120 (relative to the back gate with 285 nm SiO_2) *via* optimizing thermal oxidation of Y_2O_3

top-gate oxide. The carrier mobility in the graphene channel is significantly improved to more than 5000 $cm^2/V \cdot s$, and the transconductance normalized by dimension and drain voltage is increased to 7900 $\mu F/V \cdot s$, which is among the largest of the published graphene FETs. In an as-fabricated G-FET with L_G = 310 nm, a peak transconductance of up to 0.69 mS/μm is reached, and which may in principle be further improved by reducing the series resistance of the device. As a result of the extremely efficient gate control over the graphene channel, the Dirac point voltage of the graphene FET is shown to be designable simply by selecting suitable gate metal with appropriate work function. It is found that when changing the gate electrode from Ti to Pd the Dirac point voltage of the graphene FET can be adjusted from negative to positive, or namely, the majority of carriers in the channel at quasi-equilibrium can be changed from electrons to holes.

METHODS

Single-layer graphene samples were derived by mechanical cleavage of Kish graphite and deposited on a n-doped Si substrate with a 285 nm thermal SiO_2. Single-layer graphene samples were identified by optical contrast and Raman spectroscopy. The device fabrication is generally a gate-first process. First, a thin yttrium metal film was deposited on specific area of graphene using E-beam lithography and E-beam evaporation followed by a lift-off process. Second, an yttrium oxide layer was formed by oxidizing the yttrium film on a hot plate at 270 °C for 5 min or 180 °C for 10 min. Additional forming gas (Ar/H_2 = 5:1) annealing was carried out in a furnace at 300 °C for 1 h in order to improve the quality of the Y_2O_3 layer. Third, source/drain contacts were fabricated by E-beam lithography and E-beam evaporation followed by a lift-off process. Without specific notification, the contact metal is Ti/Au (50 nm/10 nm). Last, a 60 nm titanium or palladium gate metal was fabricated similarly to that of source/drain contacts. The device was then tested in vacuum at room temperature using a Keithley 4200 semiconductor analyzer and a probe station (Lakeshore TTP-4).

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Supporting Information Available: Additional experimental details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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